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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2138	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,299	WENDORF ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,12-16,18-21,23,26-31,34-37,40-44,47,48 and 54-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,12-16,18-21,23,26-31,34-37,40-44,47,48 and 54-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The pending claims 1-7, 9, 12-16,18-21, 23, 26-31, 34-37, 40-44, 47, 48, and 54-57 have been examined.

Response to Arguments

Applicants' arguments filed 10/31/2005 with respect to claims 1, 2, 16, and 30 have been fully considered but they are not persuasive. Applicant's arguments with respect to claims 18 and 44 have been considered but are moot in view of the new ground(s) of rejection.

Claim1:

The Applicants states that "Miner does not teach or suggest Applicants' system as it appears in amended claim 1, because in Miner, there is no memory testing engine that executes test operations on the random access memory and is embedded in a bus controller to have a memory interface shared with the memory testing engine" and "Miner does not teach or suggest that element 560 is embedded in element 570 to have a memory interface which is shared. Indeed, the two elements are connected by a bus 574 and as such are not deemed embedded within one another".

The Examiner would like to point out in the Specification as files, paragraph [0010] that "a memory testing engine (MTE) embedded on or coupled with the bus slave controller *(BSC)* on each integrated circuit". [*(BSC)* added by Examiner]. This statement implies that if the MTE and BSC were coupled together in one embodiment it would be

obvious to one skilled in the art to embed the MTE and BSC *within one another* in a second embodiment. The Examiner asserts, therefore, that it would be obvious to one skilled in the art to embed Miner's test execution logic 560 (MTE), bus controller 530 and test management logic 570 (BSC) *within one another.* Also, the Examiner can not find within the specification, in particular pages 7-11 and Fig. 3, how the MTE and BSC or UBS are embedded *within one another.* At best the specification and Fig. 3 only discloses that they are coupled, not embedded, however, it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. See *In re Larson*, 144 USPQ 347 (CCPA 1965). Further, as a result of embedding elements 560, 570 and 530 *within one another*, the Examiner asserts that Miner's memory 510 can be accessed with data traffic and test functions, passing data traffic directly to the memories, making Applicants' arguments on page 9, first paragraph moot.

It is the Examiner's conclusion that claim 1 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Also, due to their dependency on claim 1, claims 2-7, 9, 12-15 stand rejected. Therefore, the rejection is maintained.

Claim 2:

Applicants' arguments on page 9 concerning the mere duplication of various elements in Miner are fully discussed in claim 16 arguments below.

Claim 16:

The Applicant states on pages 9 and 10, "Miner does not teach or suggest that a processor transmits a number of initiation signals via **the same** *bus*, to multiple memory testing engines via multiple bus controllers, respectively" and "There is no teaching or suggestion that multiple memory test engines be added that are accessed **over the same test control bus**". Firstly, the Applicants seem to be fixated on the notion that Miner's teachings are only for a microprocessor and, as such, motivation to duplicate elements 560, 570 and 530 of Fig. 5 would not be obviousness to one skilled in the art. The Examiner disagrees and asserts Miner also teaches "Although principally designated for a microprocessor, the present invention comprehends testing of memories internal to any intelligent logic device where test parameters can be passed from a test controller to configure specific test sequences that are executed by BIST hardware within the device. Such devices include signal processors, embedded controllers, array processors, and industrial controllers". (Col. 14, ll. 55-65). Secondly, by comparing Figure 5 from Miner to Figure 2 from the instance application, the Examiner has observed that the Applicants illustrate a single BSC 250 and MTE 200 accessing a plurality of memories 260 (RAM*0*-RAM*N*) and this configuration is repeated. Miner teaches a similar configuration in Fig. 5. The Examiner asserts it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Miner's test management logic 570 (BSC), test execution logic 560 (MTE) and bus controller 530 in Figure 5 to arrive at the Applicant's invention. The artisan would have been motivated to do so since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper*

Co. v. Bemis Co., 193 USPQ 8 (7th Cir. 1977). In the duplication Normal Bus 554 and Test Bus 575 (now embedded *within one another* as per arguments presented for claim 1) would be connected to test controller 580 (via **the same** *bus*). In light of these arguments the Examiner asserts that Miner does teach that a processor (test controller 580) transmits a number of initiation signals (test parameters) via **the same** *bus* (bus 575), to multiple memory testing engines (test execution logic 560 (MTE)) via multiple bus controllers (test management logic 570 (BSC)). (Col. 10, lines 44-54).

It is the Examiner's conclusion that claim 16 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Also, due to their dependency on claim 16, claims 18-21, 23, 26-29 stand rejected. Therefore, the rejection is maintained.

Claim 30:

As per Applicant's arguments on page 10, "Applicants continue to disagree with the rejection of claim 30 as being anticipated by Miner, because Miner is directed to a single, microprocessor in which there is integrated memory and test management logic. There is no teaching or suggestion that the memory being tested in Miner is associated with an application specific integrated circuit (ASIC)". The Examiner asserts that it has already been established Miner teaches the limitation cited in claim 30 as set forth in the arguments and claim rejection of previous office action of record. In addition, the Examiner asserts that Miner teaches the testing of the memory chip 210 (ASIC) at full speed. Miner also teaches although the preceding discussion references testing of stand-alone memories (ASIC), it is now common practice to incorporate memory circuits

into a more complex integrated circuit design (again, ASIC). Miner further teaches an apparatus 500 according to the present invention for testing memory circuits 510 in a microprocessor 50 (again, testing memories within an ASIC). (Col. 6, lines 49, 64-66, col. 9, lines 62-64). Miner also teaches although principally designated for a microprocessor, the present invention comprehends testing of memories internal to any intelligent logic device where test parameters can be passed from a test controller to configure specific test sequences that are executed by BIST hardware within the device. Such devices include signal processors, embedded controllers, array processors, and industrial controllers (other ASIC devices). (Col. 14, ll. 55-65).

The Applicant also states on pages 10 and 11, "Miner does not teach or suggest that the memory testing engine be embedded in a utility bus slave (UBS) controller that is on the ASIC". The Examiner asserts that a bus controller must be present, although not explicitly disclosed, because in communicating with a test controller 580 over the test control bus 575 the test management logic 570 must include a bus controller for the management and synchronization of these bused signals. Further, Miner teaches a "utility bus" in that the present invention also anticipates such alternative embodiments wherein external logic devices in an operational configuration, say a motherboard (see Applicants arguments page 11, second paragraph "*the term "utility bus" refers to a type of back plane bus used in electronics cabinets, to receive circuit cards*"), may be used to initiate a manufacturing test mode and to provide certain parameters to executed a prescribed test within the microprocessor. (Col. 15, ll. 2-7).

Applicants arguments "Miner does not teach or suggest that a memory testing engine be embedded in the UBS controller on an ASIC" are fully covered as per the arguments for claim 1.

It is the Examiner's conclusion that claim 30 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Also, due to their dependency on claim 30, claims 31, 34-37, 40-43 stand rejected. Therefore, the rejection is maintained.

Claim Objections

2. Claim 1 is objected to because of the following informalities: The limitation "the first memory testing is embedded" on line 5 seems not to be complete. For purpose of examination the Examiner will read this as "the first memory testing engine is embedded" Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5-7, 9, 12, 13, 15, 16, 18-21, 23, 26, 27, 29-31, 34-37, 40, 41, 43, 44, 47, 48, 54, 55 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1).

Claim1:

Miner teaches the limitation cited in amended claim 1 in that the test execution logic 560 (MTE) directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed (MTE to execute test operations on the memory). Miner also teaches the test execution logic 560 sends a test signal 565 to the bus unit 530 to preclude contention on the local bus 532, thus effectively disabling the bus unit during testing 530 (if data traffic from the processor is being passed to a memory module by the first bus controller, the memory testing engine cannot run a test function). (Col. 10, lines 12-15, col. 11, lines 21-24). Miner further teaches the test management logic 570 (BSC) communicates with a test controller 580 (processor) over the test control bus 575 (bus connecting processor to BSC). Miner also teaches the test management logic 570 (BSC) interfaces to test execution logic 560 (MTE) via bus 574. Miner further teaches control logic 563 (memory controller) (note: this is part of the test execution logic 560 (MTE)) directly generates control signals over a memory control bus 564 to select and control bus a specified memory 510. (Col. 10, ll. 35-37).

Miner does not explicitly disclose "the memory testing engine is embedded ...with the first bus controller". Nevertheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine or make integral (i.e. embed) Miner's test execution logic 560 (MTE), bus controller 530 and test management logic 570 (BSC) *within one another*, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together

involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965). Further, Miner's memory 510 can be accessed with data traffic and test functions, passing data traffic directly to the memories as a result of embedding elements 560, 570 and 530 *within one another*, Miner's memory 510 can be accessed with data traffic and test functions, passing data traffic directly to the memories

Claim 30:

Miner teaches the use of a ROM 571 (machine-readable medium) for storing sequences of microinstructions and passes them from the test controller 580 (processor). Miner further discloses the test management logic 570 (bus slave controller) inserts operands into the sequence of micro instructions to form a specific sequence and then transfers the specific sequence to the test execution logic 560 (MTE) via bus 574 for perform memory testing (configuring a MTE). (See Col. 11, lines 5-20). Miner also teaches the test execution logic 560 (MTE) compares actual data obtained on a read with the expected data pattern and passes the result of each read to the test management logic 570 (bus slave controller) (processing a signal from the MTE). (Col. 11, lines 26-30). Miner teaches the testing of the memory chip 210 (ASIC) at full speed. Miner also teaches although the preceding discussion references testing of stand-alone memories (ASIC), it is now common practice to incorporate memory circuits into a more complex integrated circuit design (again, ASIC). Miner further teaches an apparatus 500 according to the present invention for testing memory circuits 510 in a microprocessor 501(again, testing memories within an ASIC). (Col. 6, lines 49, 64-66, col. 9, lines 62-64). Miner also teaches although principally designated for a

microprocessor, the present invention comprehends testing of memories internal to any intelligent logic device where test parameters can be passed from a test controller to configure specific test sequences that are executed by BIST hardware within the device. Such devices include signal processors, embedded controllers, array processors, and industrial controllers (other ASIC devices). (Col. 14, ll. 55-65). In addition, a bus controller must be present, although not explicitly disclosed, because in communicating with a test controller 580 over the test control bus 575 the test management logic 570 must include a bus controller for the management and synchronization of these bused signals.

Claim 44:

Miner teaches the limitation cited in amended claim 1 in that the test execution logic 560 (means for initiating) directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed. Miner also teaches the test execution logic 560 sends a test signal 565 to the bus unit 530 to preclude contention on the local bus 532, thus effectively disabling the bus unit during testing 530 (means for disabling the testing while passing data traffic from the initiating means to the memory over the bus). (Col. 10, lines 12-15, col. 11, lines 21-24). Miner further teaches the test management logic 570 (BSC) communicates with a test controller 580 (means for testing memory) over the test control bus 575 (bus connecting processor to BSC). Miner also teaches the test management logic 570 (means for controlling) interfaces to test execution logic 560 (means for initiating) via bus 574. Miner further teaches control logic 563 (memory controller) (note: this is part of the test

execution logic 560 (MTE)) directly generates control signals over a memory control bus 564 to select and control bus a specified memory 510. (Col. 10, ll. 35-37).

Miner does not explicitly disclose "the memory testing engine is embedded ...with the first bus controller. Nevertheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine or make integral (i.e. embed) Miner's test execution logic 560 (means for initiating), bus controller 530 and test management logic 570 (means for controlling) *within one another*, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965).

Claim 4:

Miner teaches the test execution logic 560 directly interfaces to the memories 510 and to the bus controller 530.

Claims 5 and 47:

Miner teaches the test execution logic 560 executes test sequences of data patterns to write and expected data patterns to read. (See col. 10, lines 49-54, col. 11, lines 12-18).

Claims 6, 34 and 48:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 27-29).

Claims 7 and 36:

Miner teaches the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test

management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18).

Claim 35:

Miner teaches the test sequences that are designed into the test management logic 570 can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. In addition, a test sequence can be configured to repeat a specified number of times before it completes. (See col. 10, lines 49-56). Miner also teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 26-28).

Claims 12,13, 40, 41, 54 and 55:

Miner teaches that the result of each read, containing a bit-by-bit result, is provided to the test management logic 570 via bus 574. The result is placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 28-31 and col. 10, lines 56-60).

Claim 16:

Miner teaches that test management logic 570 (bus slave controller (BSC)) receives test parameters (initiation signals) from the test controller 580 (processor) to execute access to any memory (accessing memories) via the test execution logic 560 (MTE) via bus 574. (Col. 10, lines 44-54). Miner teaches in Figure 5 a single BSC and MTE accessing a plurality of memories. Miner also teaches the test execution logic 560 (MTE) directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed (MTE to execute test operations on the memory). Miner further teaches the test execution logic 560 sends a test signal 565 to the bus unit 530 to preclude contention on the local bus 532, thus effectively disabling the bus unit during testing 530 (passing control data, address and control pathways...so that only one of the two has control at one time). (Col. 10, lines 12-15, col. 11, lines 21-24). Miner even further teaches control logic 563 (memory controller) (note: this is part of the test execution logic 560 (MTE)) directly generates control signals over a memory control bus 564 to select and control bus a specified memory 510. (Col. 10, ll. 35-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Miner's test management logic 570 (BSC) and test execution logic 560 (MTE) in Figure 5. The artisan would have been motivated to do so since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

Claims 2:

Miner does not explicitly teach of a second memory test engine to test a second random access memory. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the teaching of Miner can be duplicated to include a second test execution logic and test management logic entities to perform a similar function.

Claims 9, 23 and 37:

Miner teaches the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18). Miner does not explicitly disclose that the address is decremented, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the configurable test sequences within the test management logic 570 that can access to any memory 510, within any address range, in an incrementing order can also decrement the address in testing the memory. The artisan would be motivated to do so since it is common practice in testing memories to decrement as well as increment the address locations.

Claim 18:

Miner does not explicitly disclose "transmitting data traffic from the processor through the bus to one of the random access memories via the data, address and control pathways while such are under control of the respective bus controller". Nevertheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine or make integral (i.e. embed) Miner's test execution logic 560 (means for initiating), bus controller 530 and test management logic 570 (means for controlling) *within one another*, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965). The artisan would be motivated to do so because Miner's interfaces would then be shared (normal bus 554 and control bus 575) and the non-test functions (data traffic) could be performed through the shared bus.

Claim 19:

Miner teaches the test execution logic 560 executes test sequences of data patterns to write and expected data patterns to read. (See col. 10, lines 49-54, col. 11, lines 12-18).

Claim 20:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 27-29).

Claim 21:

Miner teaches the test sequences that are designed into the test management logic 570 can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. In addition, a test sequence can be configured to repeat a specified number of times before it completes. (See col. 10, lines 49-56). Miner also teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 26-28).

Claims 26 and 27:

Miner teaches that the result of each read, containing a bit-by-bit result, is provided to the test management logic 570 via bus 574. The result is placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 28-31 and col. 10, lines 56-60).

Claims 15, 29, 43, 57:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern. Any detected defects are represented by a mask bit (logical "1") and placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 24-31, 44, 45). It would have been obvious to one of ordinary skill in the art at the time the invention was made that the mask bit set in the result register alerts the test controller of the mismatch and alters operation.

Claim 31:

Miner does not explicitly teach of a plurality of memory test engines to test a random access memory. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the teaching of Miner can be duplicated to include a plurality of test execution logic and test management logic entities to perform a similar function. The artisan would have been motivated to do so because duplicate parts for multiple effects depend on the necessity of time saving for testing the memories.

4. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Satoh (US-6501690 B2).

Claims 3:

Miner does not explicitly teach that the test execution logic performs testing concurrently. However, Miner does teach the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18). Satoh teaches of a method for diagnosing a

memory array including a plurality of memory banks, which can independently read/write data by writing identical data in parallel. This method also reads out storage data and compares the data read out to the data that was written. According to the above method, the memory including the plurality of banks can be diagnosed at one time or concurrently. (See col. 1, 43-48, 54, 55). Satoh also teaches the memory diagnostic circuit controls the memory banks to collectively write data at one time, and the comparison circuit compares the written data and the data from the memory banks. In this structure, the plurality of memory banks can be diagnosed at one time. (See col. 2, lines 6-12). Also, in the memory diagnostic circuit 11 of this embodiment, the plurality of memories 14a to 14d, which are divided into four memory banks, can collectively be diagnosed at one time. (See col. 5, lines 65-67, col. 6, line 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to "reconfigure" the test sequences within the test management logic of Miner to test the memories concurrently in view of the teachings of Satoh. Specifically, the control logic within the test execution logic directly generates control signals over a memory control bus to select and control a specified memory. The artisan would have a motivation to do so because Miner suggests that the test controller can access many memories (see col. 10, lines 49-54) which would be more than one memory.

5. Claims 14, 28, 42, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Chambers et al. (US-20020078408 A1).

Claims 14, 28, 42, 56:

Miner teaches that the test controller 580 generates a defect map and determine the correct way to repair the array. (Col. 10, lines 58-60). Chambers teaches of an error register which indicates that when errors exist, the computer system interrogates the error register at step 1120 and retrieves the stored contents of the read registers (step 1130). At this point, the test procedure terminates in a FAIL (step 1150). (Page 3, paragraph 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made that to terminate the testing procedure upon encountering an error to create a defect map. The artisan would have been motivated when creating the defect map of Miner the test procedure would terminate in a fail as taught in Chambers.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 1/18/06
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100